

*C24* internal circuit forms a current path, and a feedback circuit between the gate of said first MOS transistor and the output of said first circuit. --

**REMARKS**

Applicants' Attorney, the undersigned, the inventor Mr. Itoh and applicants Japanese representative Mr. Uchigiri wish to thank Examiner Baker for the courteously extended during the interview of November 21, 1995. Based on the discussions held during the interview the present Amendment is being filed.

As discussed during the interview modifications were made to the specification to emphasize the fact that as disclosed the present invention is intended to replace the conventional voltage converter 13 as illustrated in Figs. 1 and 2 of the present application. Also amendments were made to the specification as discussed during the interview to clarify as illustrated in Fig. 16 that the conductance of the MOS transistor  $Q_f$  is controlled by the output voltage  $V_L$  via feedback of the output voltage  $V_L$  through MOS transistors  $Q_1 \dots Q_i \dots$ , and  $Q_n$  to the gate of MOS transistor  $Q_f$ .

The above-noted amendments to the specification are reflected in the substitute specification which is now being prepared as requested by the Examiner in paragraph 1 of the Office Action. The substitute specification will be filed as soon as completed.

The drawings stand objected to due to various informalities noted by the Examiner in paragraph 2 of the Office Action. Filed herewith are Proposed Drawing Corrections to correct the informalities noted by the Examiner. Therefore, this objection is overcome and should be withdrawn.

Claims 7-125 stand rejected under 35 USC §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Various were amendments were made to claims 7-125 to bring them into conformity with 35 USC §112, second paragraph. Therefore applicants submit that this objection is overcome and should be withdrawn.

During the interview discussions were held concerning the language used in the claims, namely, "small dependence" and "large dependence". As agreed during the interview applicants can be their own lexicographer and can describe the invention in any terms applicants so desire so long as the terms are not misused or used in a manner contrary to the well accepted meaning of the terms. The terms "small dependence" and "large dependence" correspond to the description of the present invention on page 18, lines 6-12 and 13-19 wherein with respect to the features of the present invention illustrated in Figs. 16 and 17 relationships are described between  $V_{cc}$  and VL. Thus it is applicants' contention and as agreed during the interview the claims as written with the above-noted terms or with

similar terms adequately describes the features of applicants' invention so as to apprise one of ordinary skill in the art meets and bounds of the claims.

Further to the 35 USC §112, second paragraph rejection the Examiner objected to the language used in claim 8. Particularly, the Examiner alleges that the term "feedback circuit" is misdescriptive. This feature of applicants' invention is clearly illustrated in Fig. 16 as being a feedback between  $V_L$  through MOS transistors  $Q_1 \dots Q_i \dots$ , and  $Q_n$  and the gate of the first MOS transistor  $Q_1$ . Amendments were made to the specification to clarify this feature. Therefore, the term "feedback circuit" as used in claim 8 is not misdescriptive of the invention as illustrated in Fig. 16.

Still further, to the 35 USC §112, second paragraph rejection the Examiner objected to claim 33 being that the Examiner alleges that the "fourth circuit" now recited in the claims as the third circuit is not apparent from the specification. The third circuit as now recited in claims 33, 62, 90 and 116 corresponds to the interface circuit B as illustrated in Fig. 2 of the present application. Such an interface circuit B is provided in a semiconductor integrated circuit, wherein the conventional voltage converter 13 is replaced by the voltage converter of the present invention.

Still further yet, to the 35 USC §112, second paragraph rejection the Examiner objected to the phrase "a larger

thickness of a gate insulator" recited in claim 36. The larger thickness of a gate insulator as recited in claim 36 corresponds to the difference in thickness in the gates illustrated in Fig. 2 of the present application. As discussed during the interview the present application provides a voltage converter which replaces the conventional voltage converter 13 illustrated in Fig. 2. Thus the difference in thickness of the gate insulators of the interface circuit B and circuit A would remain the same and therefore would form a part of the invention defined in claim 36.

Various other amendments were made throughout the claims to more clearly describe features of the present invention and to bring the claims into conformity with the requirements of 35 USC §112, second paragraph.

The Examiner's cooperation is respectfully requested to contact Applicants' Attorney by telephone if any further indefinite matter is discovered so that appropriate amendments may be made.

In light of above applicants respectfully request the Examiner to reconsider and withdraw 35 USC §112, second paragraph rejection.

Claims 7-125 stand rejected under 35 USC §103 as being unpatentable over Yoshioka. As indicated above claims 32, 74 and 89 were cancelled. This rejection with respect to claims 7-31, 33-73, 75-88 and 90-125 is traversed for the following reason. Applicants submit that the features of

the present invention as now recited in claims 7-31, 33-73, 75-88 and 90-125 are not taught or suggested by Yoshioka whether taken individually or in combination with any of the other references of record. Therefore, applicants respectfully request that the Examiner reconsideration and withdraw this rejection.

During the interview an English language translation of the Yoshioka reference was provided to the Examiner.

Another copy of the English language translation of Yoshioka is attached herewith for the Examiner's reference.

As discussed during the interview Yoshioka merely discloses a linearizer circuit which is a signal converter for linearizing a non-linearizer electrical output of the detector element of a detector. As taught in Yoshioka the linearizer circuit is used for linearizing the non-linear electrical output signal of a detector which is used to detect some physical phenomena. The detector may be a thermocouple or other such device.

As taught in Yoshioka if for example the detector element is a thermocouple a temperature-electromotive force curve corresponding thereto would exhibit a maximum of about 10% non-linearity. In other words the thermocouple would output a non-linear electrical signal having an S-shaped characteristic which is illustrated for example in Fig. 5 of Yoshioka. The linearizer circuit taught by Yoshioka takes the non-linear output signal of the thermocouple and makes it as close as possible a linear signal.

The above described features of Yoshioka do not teach or suggest the features of the present invention as recited in the claims. Particularly the claims of the present application provides a converter circuit used on a semiconductor integrated circuit having first and second circuits wherein the second circuit is used to perform an aging test of the semiconductor integrated circuit. Such an aging test of a semiconductor integrated circuit using first and second circuit as recited in the claims of the present application are not taught or suggested by Yoshioka.

Therefore, as discussed during the interview the above noted rejection of claims 7-31, 33-73, 75-88 and 90-125 should be reconsidered and withdrawn.

New claims 126 and 127 were added directed to a semiconductor integrated circuit including the above noted features shown not to be taught or suggested by Yoshioka. Thus, the same arguments as stated above apply to claims 126 and 127. Accordingly, the features of claims 126 and 127 are not taught or suggested by Yoshioka whether taken individually or in combination with any of the other references of record.

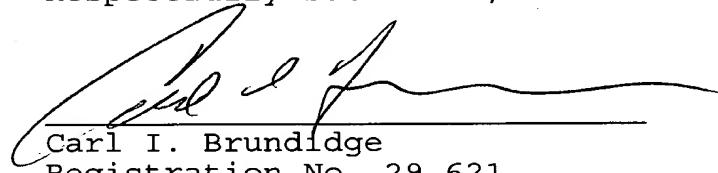
The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references and utilized in the rejection of claims 7-125.

In view of the foregoing amendments and remarks applicants submit that claims 7-31, 33-73, 75-88 and 90-127

are in condition for allowance. Accordingly, early allowance of these claims is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 C.F.R. section 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (Case No. 501.20699VC3) and please credit any excess fees to such Deposit Account.

Respectfully submitted,



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